IN THE CLAIMS

Please amend the claims as follows:

Please rewrite claim 1 as follows:

1. (Amended) An apparatus for generating an interrupt, said interrupt being requested by an assertion of an interrupt request signal, [and] said apparatus comprising:

means for indicating a software condition;

means for indicating a hardware condition; and

means for generating said interrupt in response to the assertion of said interrupt request signal, said means for generating responsive to said indicated software condition and said indicated hardware condition.

Please rewrite claim 12 as follows:

12. (Amended) A method for generating an interrupt, said interrupt being requested by the assertion of an interrupt request signal, said method comprising the steps of:

indicating a hardware condition;

indicating a software condition; and

generating said interrupt in response to said interrupt request signal, said step of generating dependent upon said indicated software condition and said indicated hardware condition.

Please cancel claims 19-22, without prejudice.

Please add the following new claims 23-26:

-- 23. In a processor that may enter a certain state from which it may only escape via an interrupt, and in which certain state all interrupts may be masked, and further in which certain state no interrupt may be unmasked conventionally, a circuit for overriding a masked interrupt, said current comprising:

a first subcircuit that provides a first signal to enable conventional unmasking, which first signal would be ineffective alone to effect unmasking when said processor is in said certain state;

a second subcircuit that provides a second signal that indicates that said processor is in said certain state; and

a third subcircuit, responsive to said first signal and said second signal, and further responsive to an interrupt request signal, for generating an interrupt request.

24. A circuit as recited in claim 23, wherein said certain state is an idle state.

25. A circuit as recited in claim 23, wherein said third subcircuit comprises an AND gate.

26. A circuit as recited in claim 23, wherein said first signal and said second signal can assume various states; and wherein when said second signal is in one particular state, said second signal alone, notwithstanding the state of said first signal, can cause said third subcircuit to generate an interrupt signal. --

REMARKS

Favorable reconsideration of the above-identified application, as presently amended, is respectfully requested.